REMARKS

Claims 1-20 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Turning now to the art rejection, Claims 1-5, 8-15, and 18-20 were rejected under 35 U.S.C. § 103 as being unpatentable over Bjerede in view of Hafez; Claims 7 and 17 were rejected under 35 U.S.C. § 103 as being unpatentable over Bjerede in view of Hafez and further in view of Boesch; and Claims 6 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over Bjerede, Hafez in view of Khlat.

These rejections are respectfully traversed.

It is respectfully submitted that Bjerede does not disclose or suggest the presently claimed invention including the first frequency synthesizer coupled to the second input of the IF processor for providing the first combining signal of one of a plurality of possible frequency separated from one another by a raster component of the desired frequency channel spacing in independent Claim 1, albeit defined as combining the first combining signal with a baseband signal to produce a IF signal in independent Claim 11.

The Examiner alleges that Bjerede discloses the first frequency synthesizer at element 100 in Figure 9.

The Examiner's attention is directed to column 15, lines 15-25 of Bjerede where Bjerede discloses that all of the frequencies generated by local oscillator 100 and the frequencies of the signals provided to mixer 106 and the baseband processor 26 are all integer multiples of 9.6.

Additionally, the Examiner's attention is directed to column 8, lines 50-55 where Bjerede discloses that the intermediate frequency signal is provided to IF processor 28.

Consequently, one can see that the oscillator 100 does not provide signals to IF processor 28.

Only the baseband frequency is supplied to processor 26 not the first combining signal.

Additionally, whether or not Hafez discloses a phase lock loop and whether or not one would consider modifying Bjerede is of no moment since the resulting construction would still in no way disclose or suggest the presently claimed invention.

Further, whether or not Boesch teaches phase lock loop synthesis or whether or not one of ordinary skill in the art would consider modifying Bjerede is of no moment since the resulting construction would still in no way disclose or suggest the presently claimed invention.

Whether or not Khlat discloses a PLL frequency synthesizer and whether or not Bjerede could be modified is of no moment since the resulting construction would still in no way disclose or suggest the presently claimed invention.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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